Figure 1 - DT/IT processes up to IT CMP
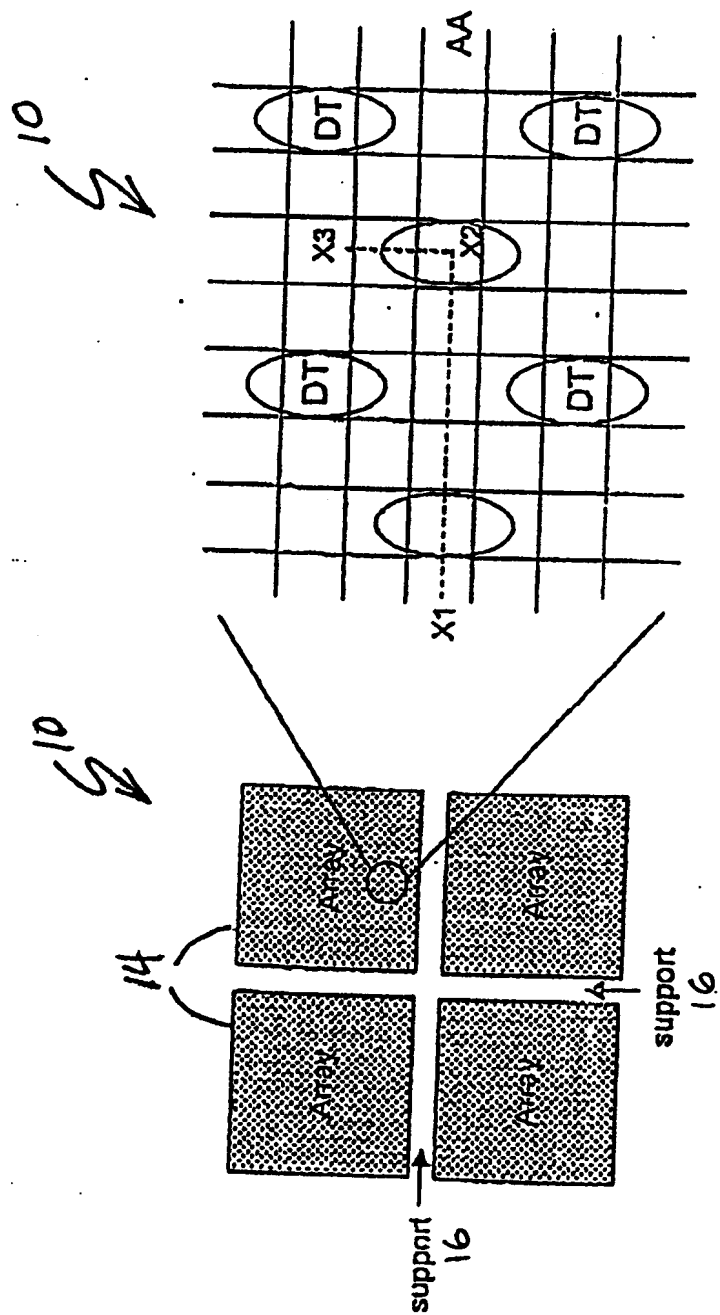
Support Area

Pad oxide 18

14 16

Array Area

52

12

X1

X2

X3

Pad nitride 30

IT (Isolation Trench)

Figure 2 – Top down view of Figure 1

10

14

support
16

support
16

X1

X3

X2

DT

DT

DT

DT

AA

10

Support Area

Array Area

X1   X2   X3

Oxide hard mask 36

Nitride liner 34

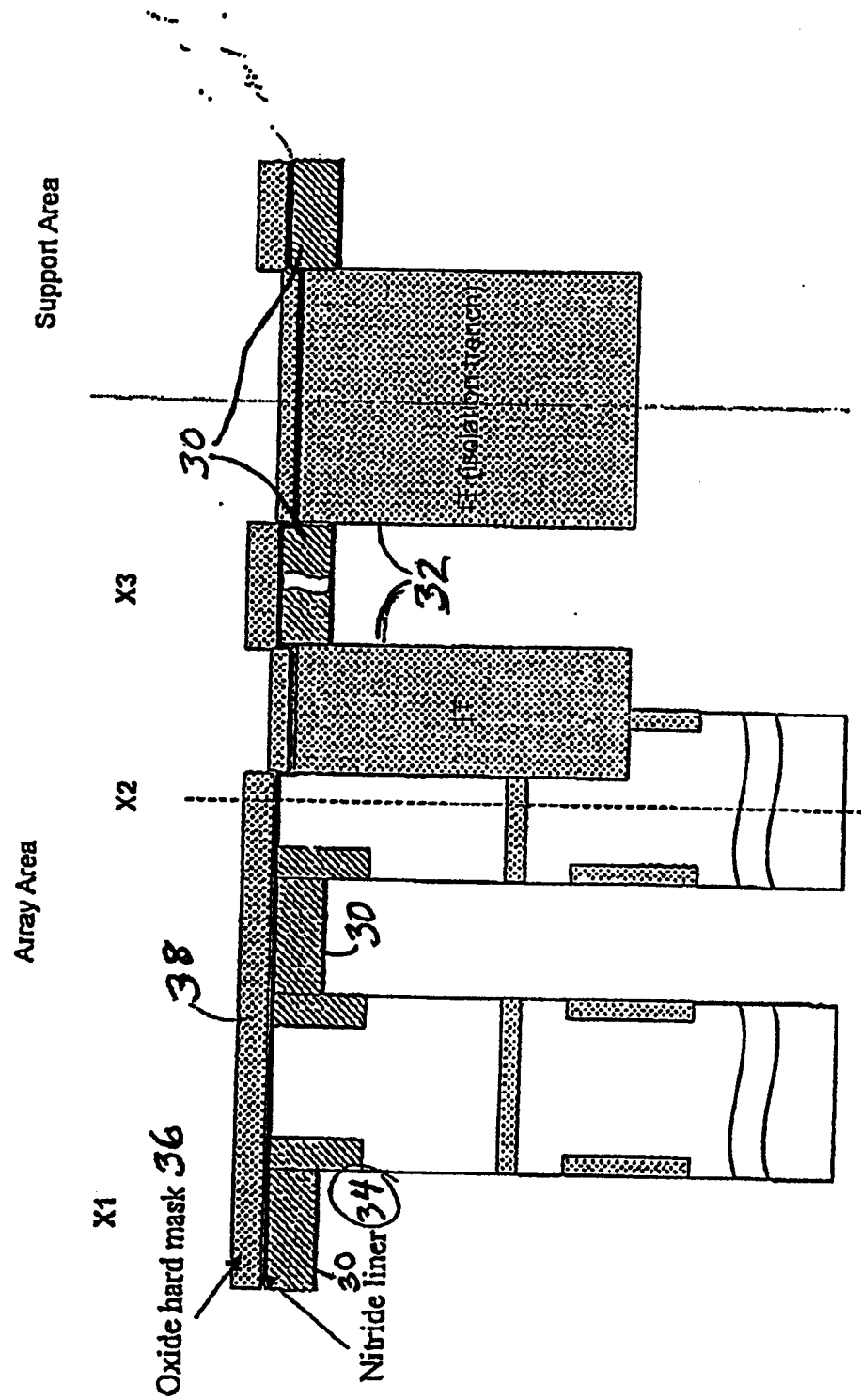Nitride liner

30   38   30   32   30

Si (isolation trench)
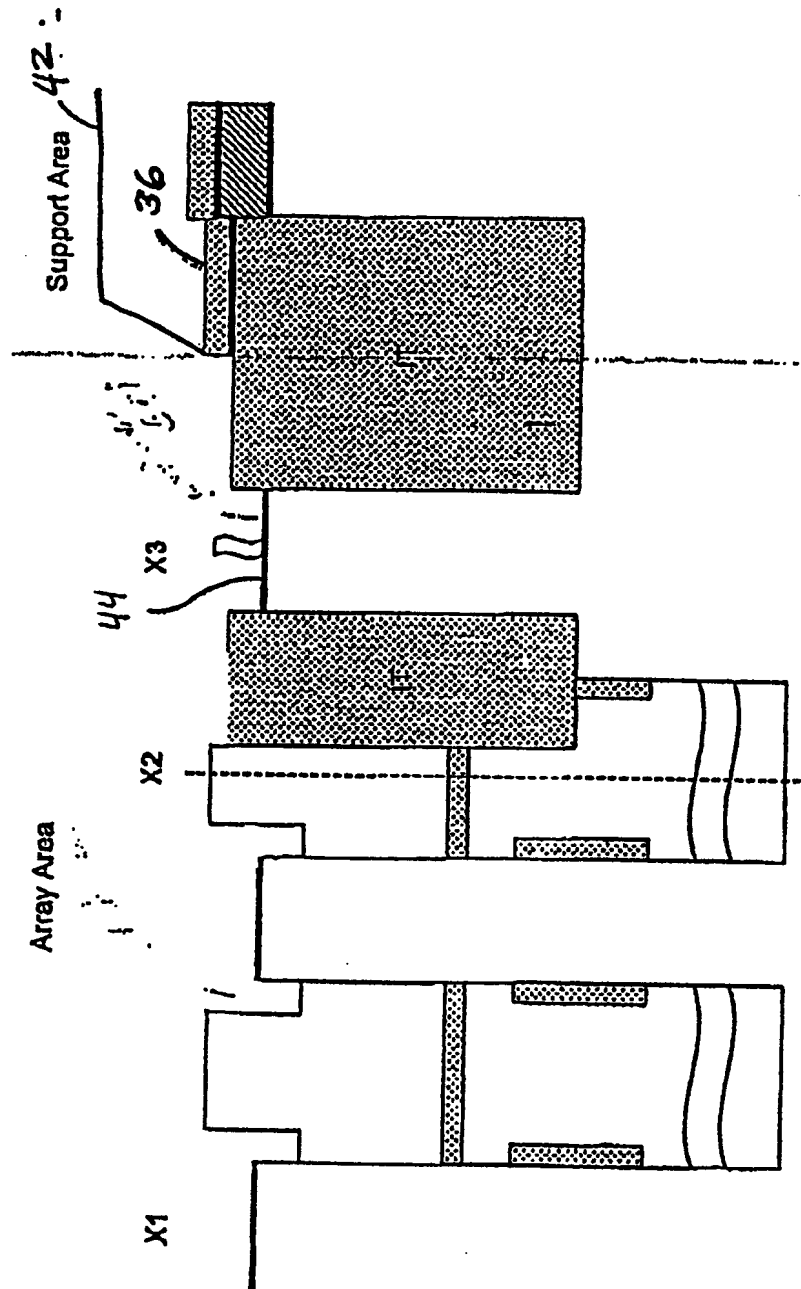
Figure 3 – Deglaze/Nitride liner dep (optional)/Oxide mask dep

Figure 4 - BA litho (block mask)/oxide etch in array/resist strip/Nitride liner, nitride spacer & pad nitride strip in array/Pad oxide strip in array/Pad oxide strip/regrow pad oxide

Support Area

Array top oxide

58

Oxide hard mask 36

54 34

Array top oxide

X3

32

X2

Array Area

Diffusion area 55

X1

Array top oxide 56

52 Nitride spacer

Optionally nitride liner 54 can be deposited to fill possible defects in nitride spacers or isolation trenches
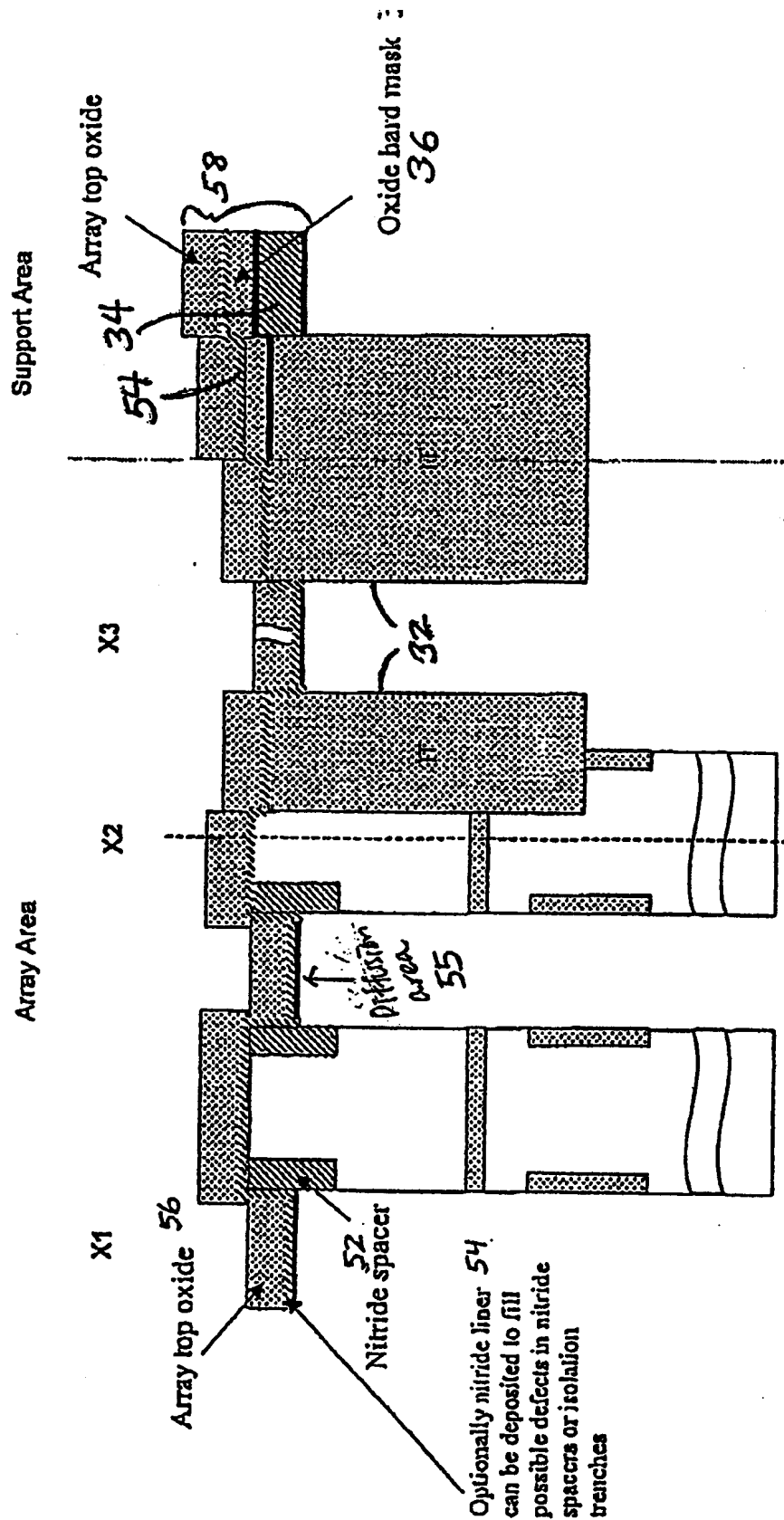
Figure 5 - Nitride spacer dep & etch/Array implants/
Nitride liner dep to fill possible defects in nitride spacer or 1T (optional)/Array top oxide dep
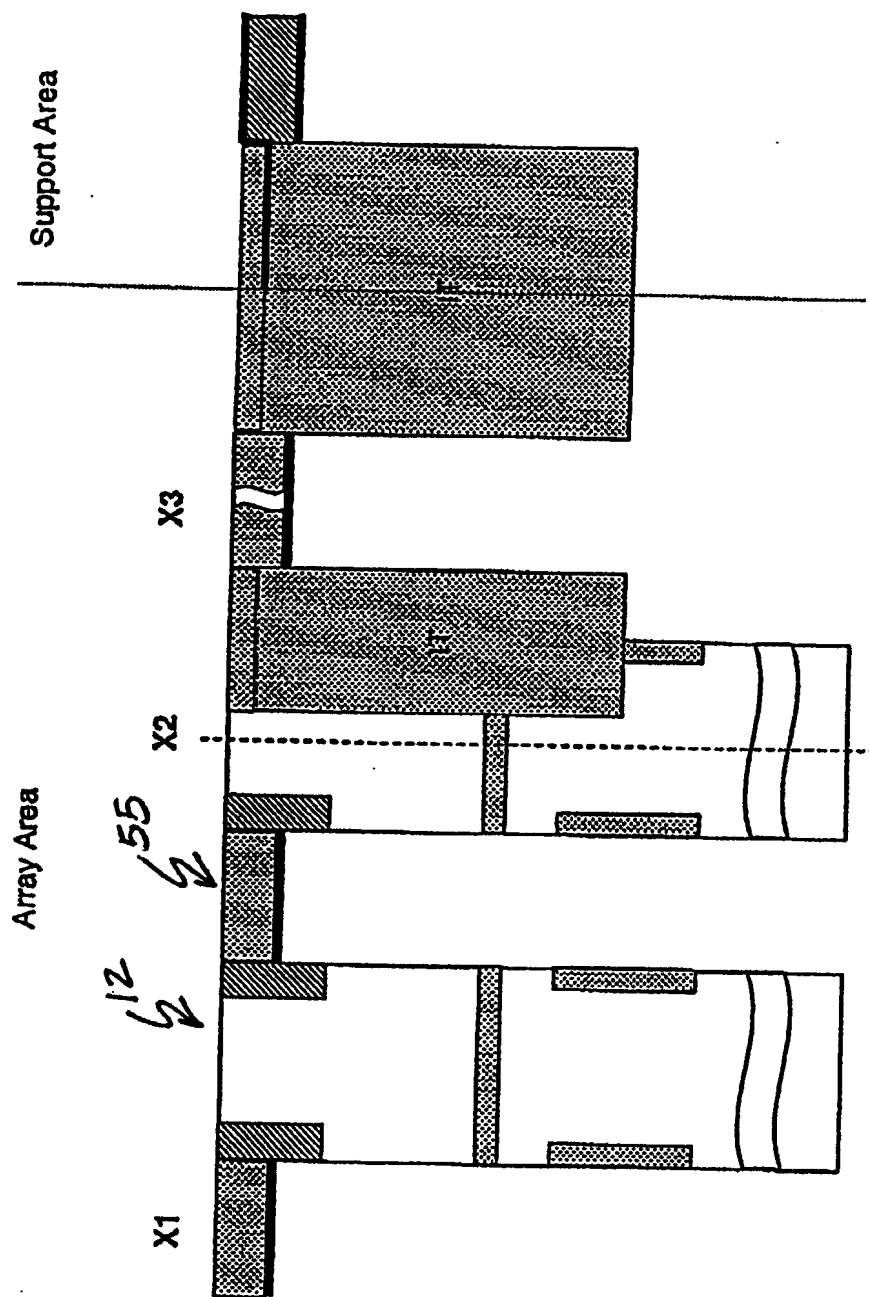
Support Area

Array Area

X1

X3

X2

12
55

Figure 6 - ATO CMP (or ARC planarization)

Figure 7 - Poly dep/ES litho/poly etch in support/resist strip

Support Area

Array Area

Block mask

72
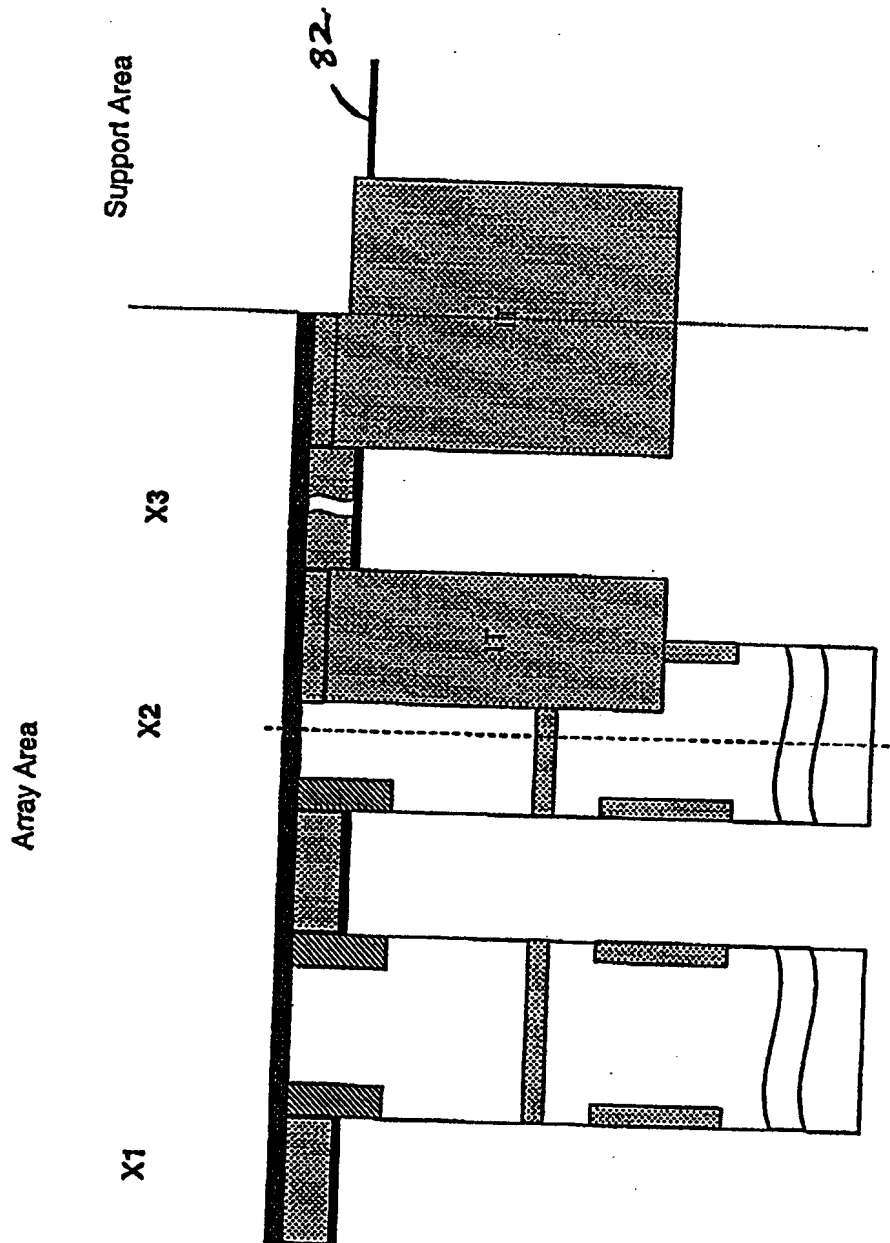
X3

X2

X1

Poly hard mask 70

Figure 8 - Etch oxide, nitride liner & IT oxide to a desired height/Strip pad nitride in support/Pad oxide strip & sac ox growth in support/Support implants

Support Area

Array Area

94
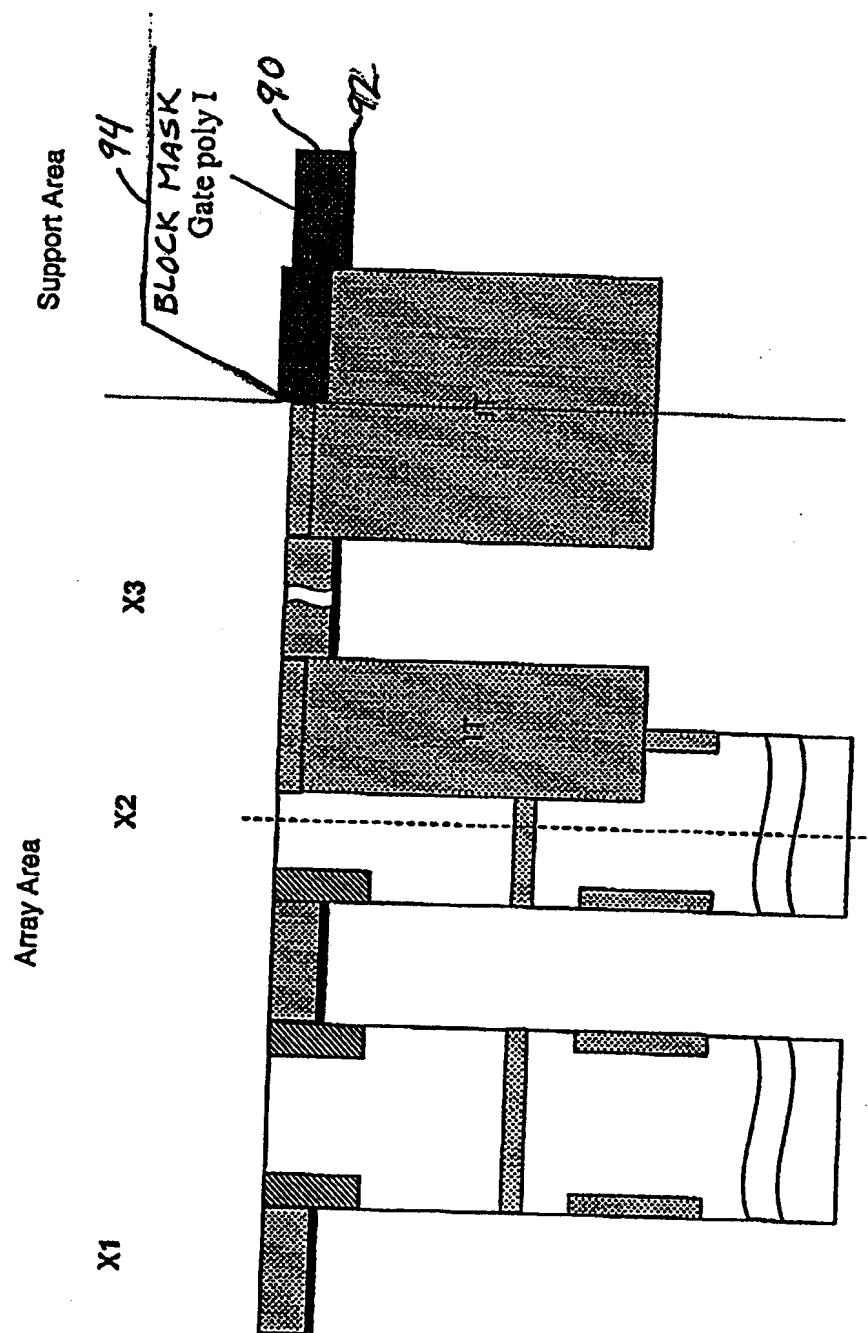
BLOCK MASK

Gate poly I

90

92

X1

X2

X3

Figure 9 - Gate ox/WL's/BL's formation and BEOL processes

Support Area

Array Area

X3

X2

X1

105
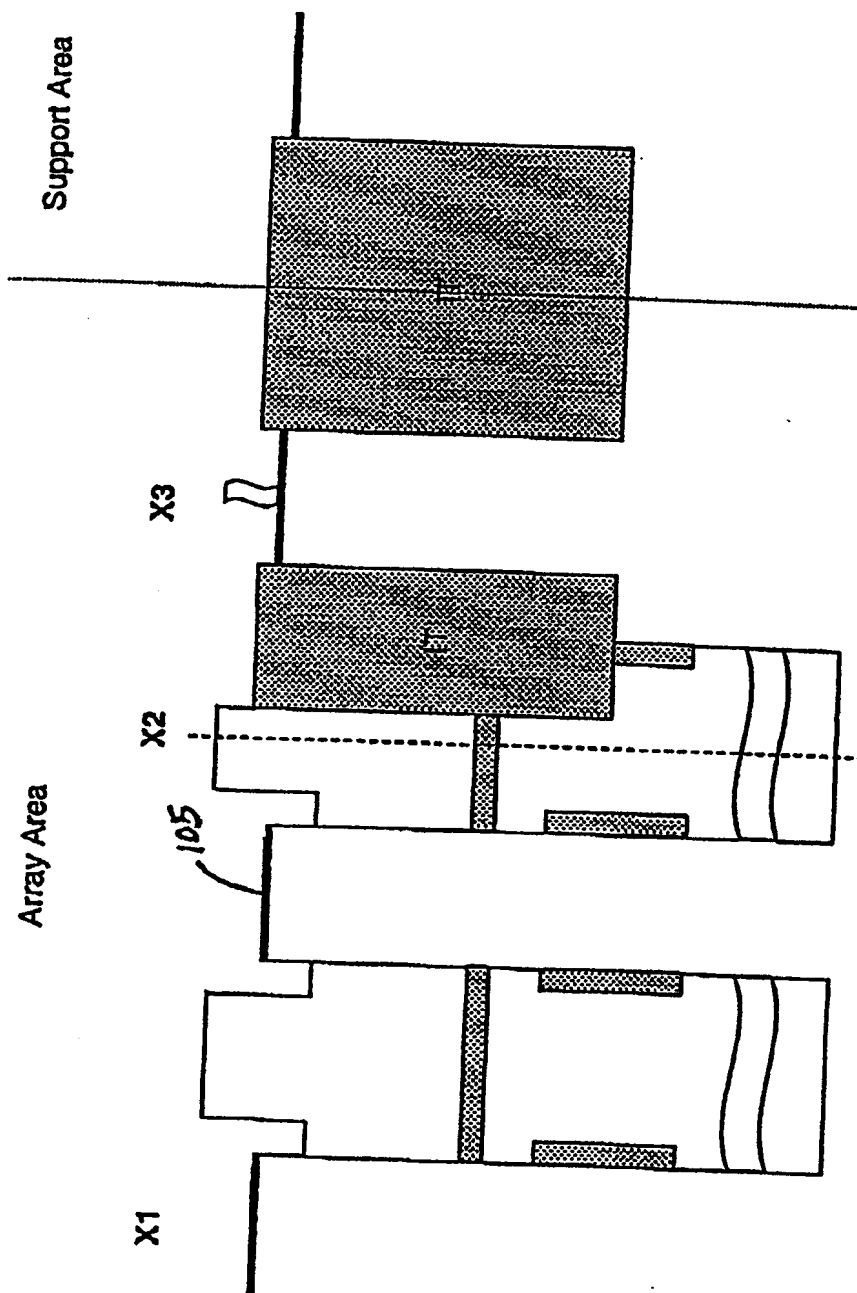
Figure 10 – Deglaze/Pad nitride strip/Pad oxide strip/pad reox

Support Area

X3

Array Area

X2

X1

114

110

TON (top oxide nitride) liner
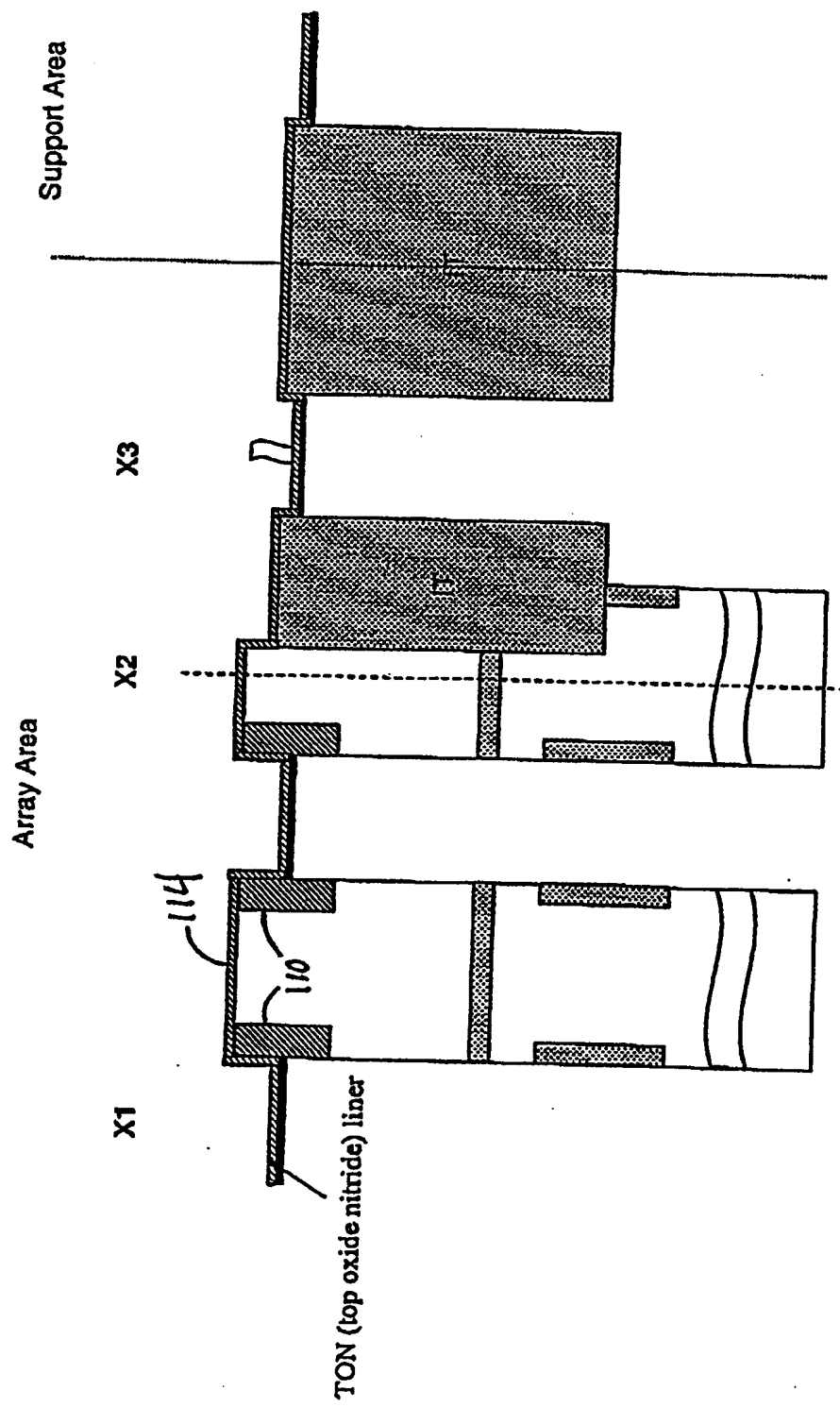
Figure 11 – Nitride spacer formation/Array implants/TON liner

Support Area

Array Area

X1

X2

120

X3

Array top oxide (ATO) dep

Figure 12 Array top oxide dep

Support Area

Array Area

Planarizing ARC dep

X1

130

X2

X3
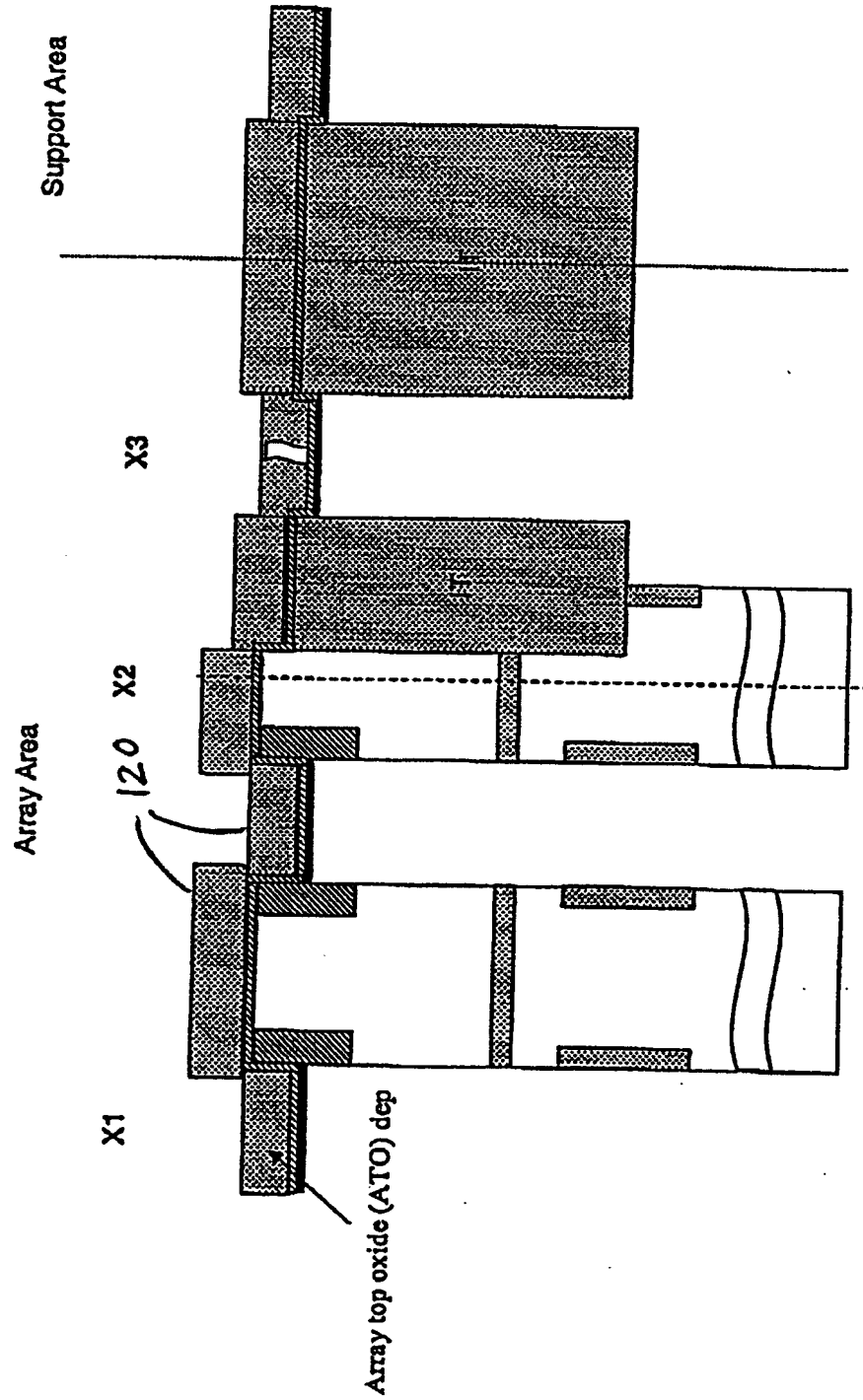
Figure 13A-Planarizing ARC dep

Array Area

Support Area

X1   X2   X3

12   55

ARC planarization (ARC dep & non-selective RIE) replaces chemical mechanical polishing.
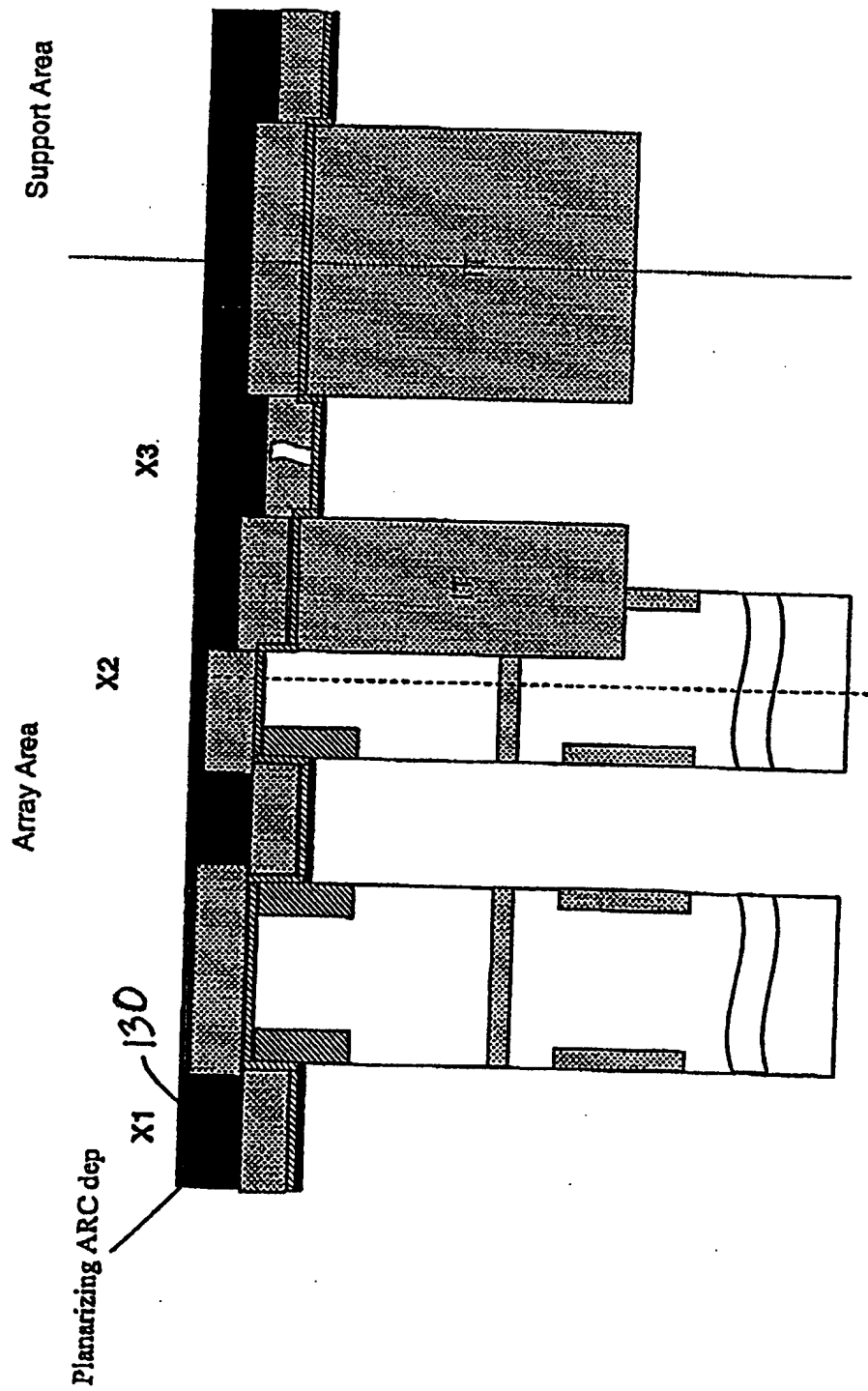
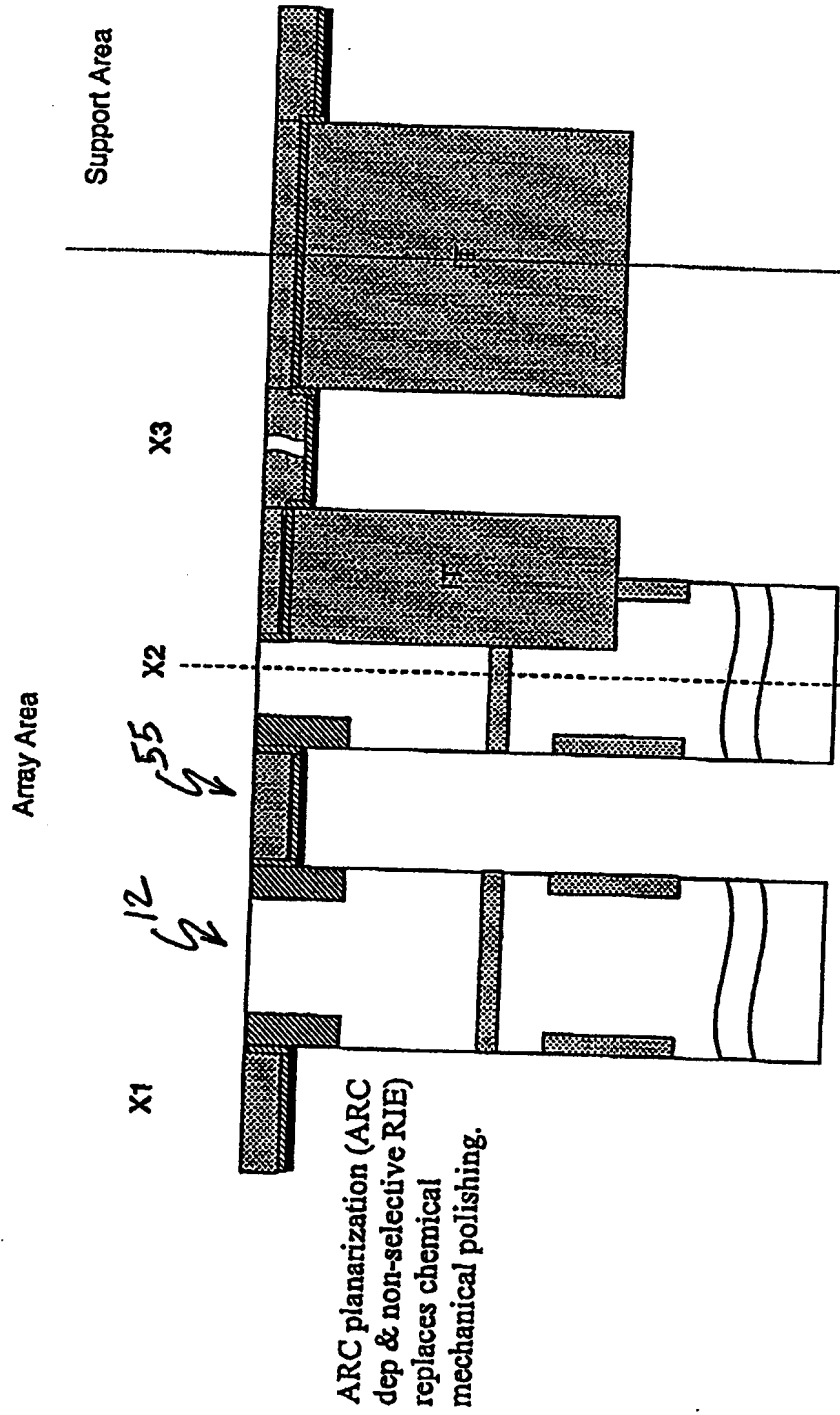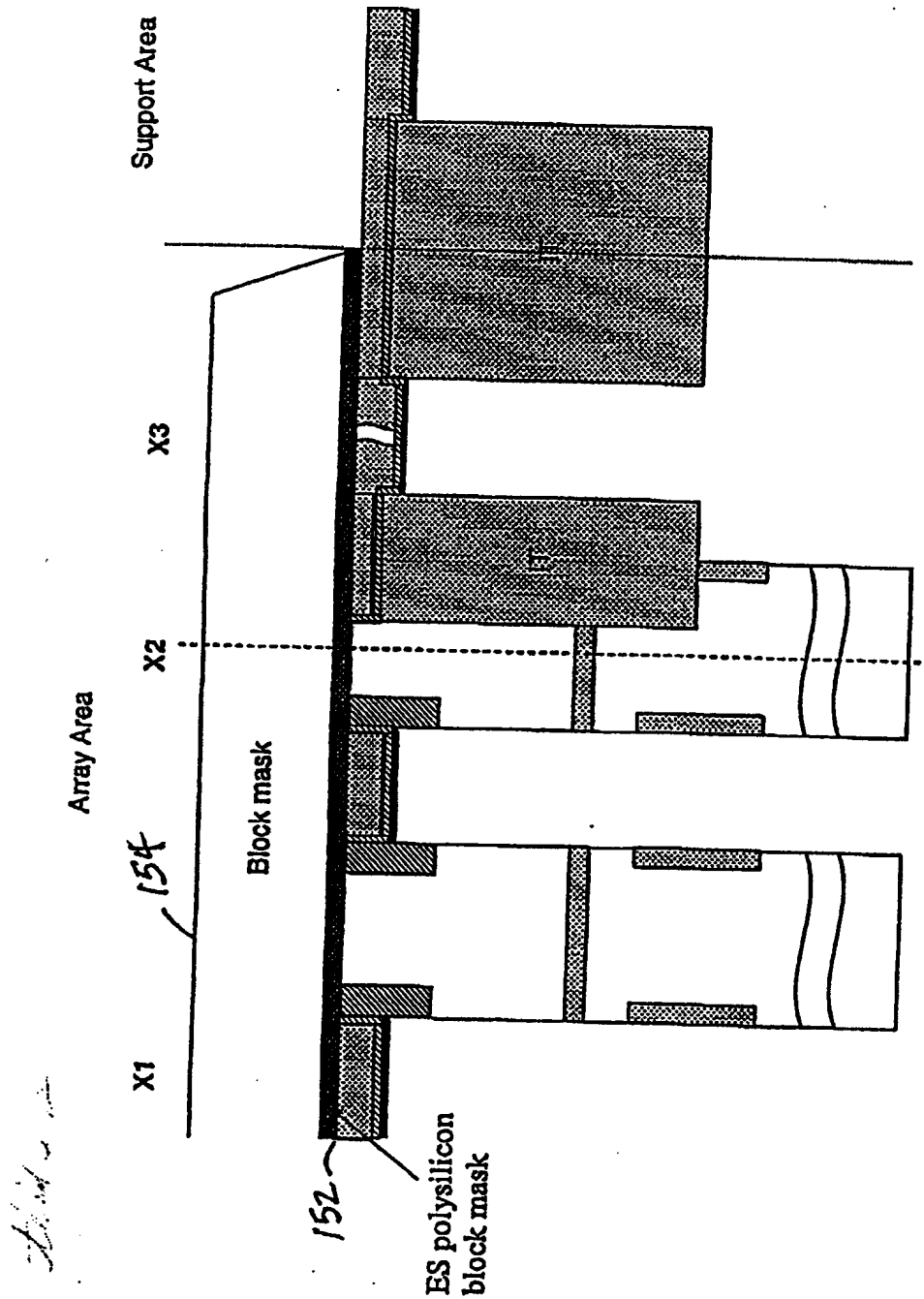Figure 14A·Non-selective RIE to remove oxide on DT stud

Figure 14b- ES poly dep/block mask/poly etch in support/resist strip/ Continue with gate conductor/WL/BL/BEOL formation.

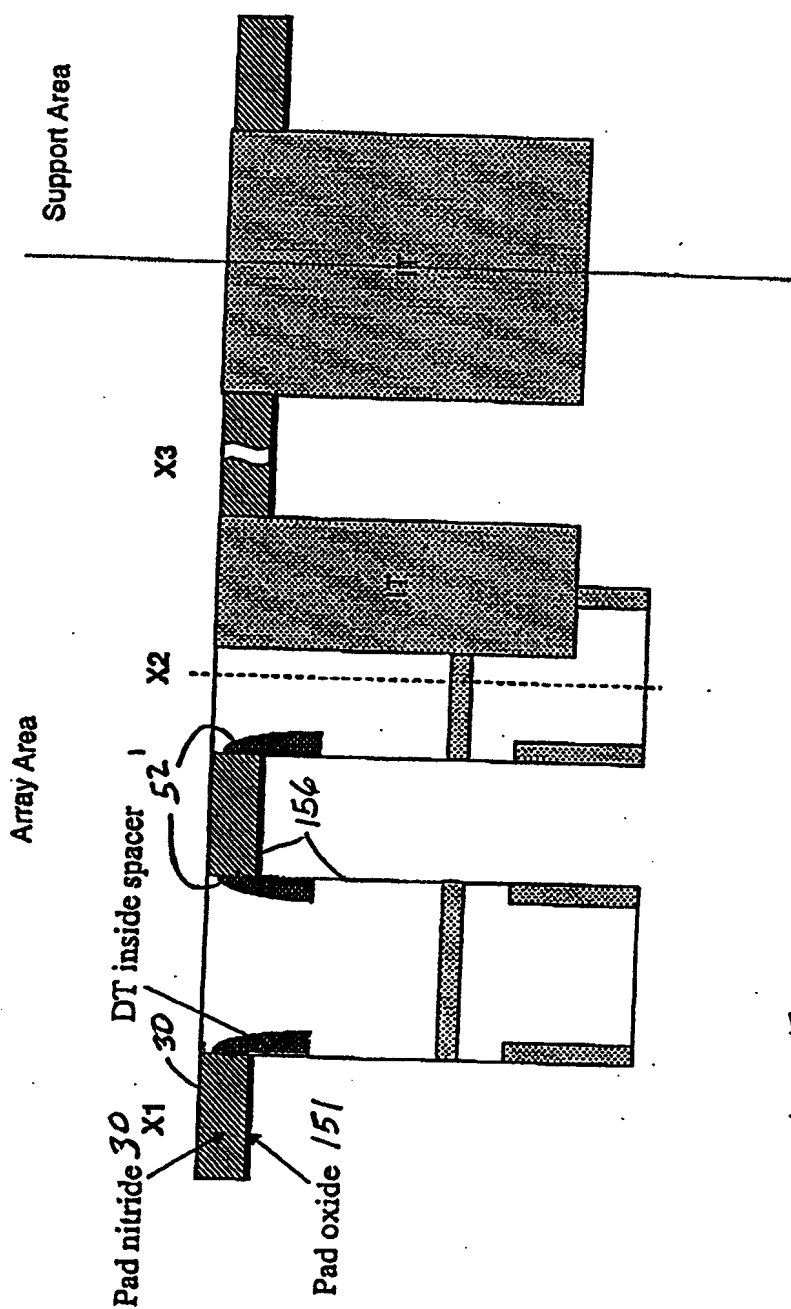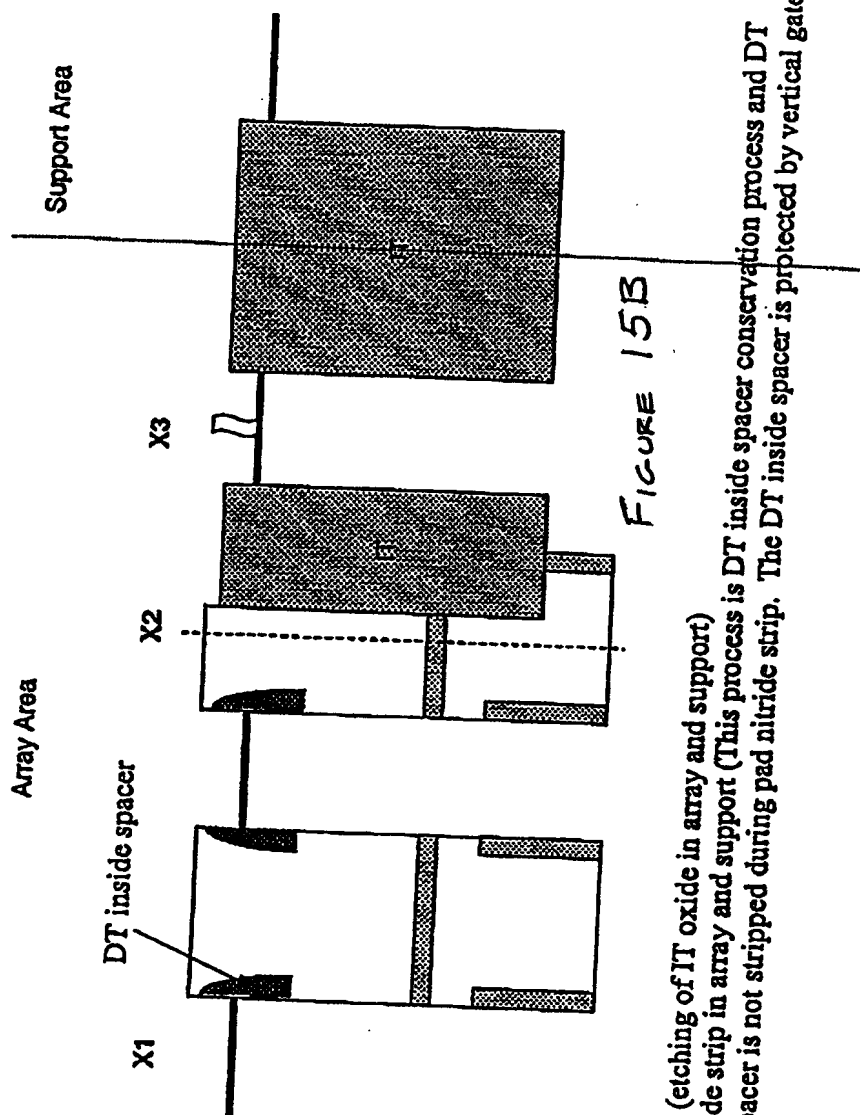Schematics of TOL with ARC planarization & height equalization between array and support

Array Area

Support Area

Pad nitride 30
X1

DT inside spacer

30

52

156

Pad oxide 151

X2

X3

FIGURE 15A – DT and IT processes up to IT CMP

Schematics of TOL with ARC planarization & height equalization between array and support

Array Area

Support Area

X1

DT inside spacer

X2

X3

FIGURE 15B

Deglaze (etching of IT oxide in array and support)
Pad nitride strip in array and support (This process is DT inside spacer conservation process and DT
inside spacer is not stripped during pad nitride strip. The DT inside spacer is protected by vertical gate
oxide.)

Schematics of TOL with ARC planarization & height equalization between array and support

FIGURE 15C
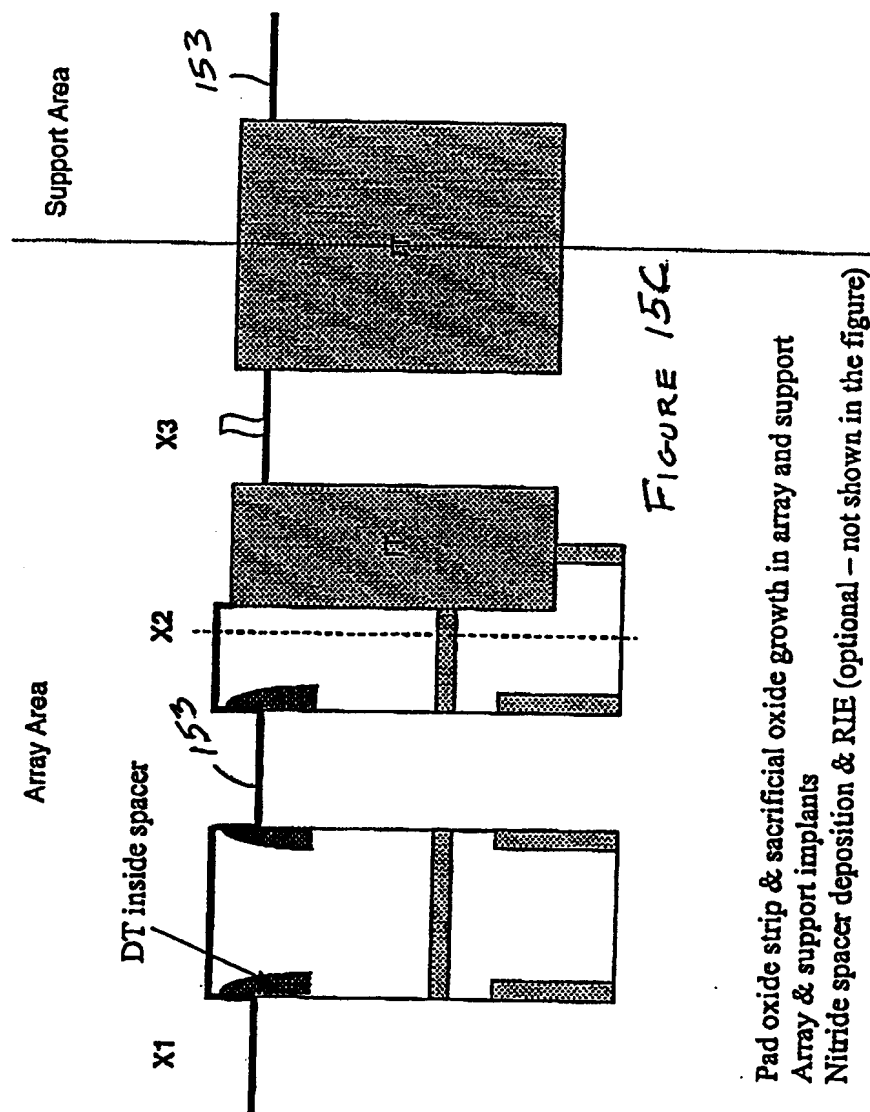
Pad oxide strip & sacrificial oxide growth in array and support
Array & support implants
Nitride spacer deposition & RIE (optional – not shown in the figure)

Schematics of TOL with ARC planarization & height equalization between array and support

Array Area

Support Area 159

Block mask 157

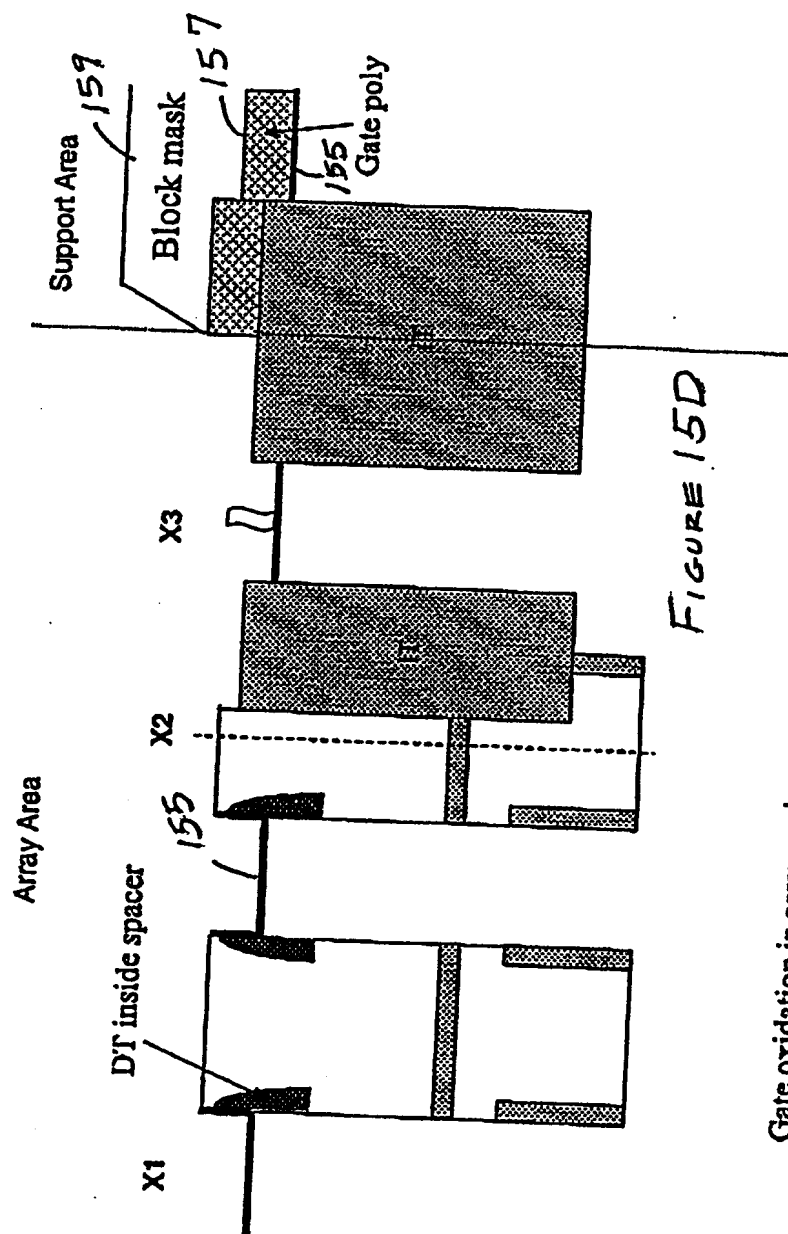155 Gate poly

DT inside spacer

X1   155   X2   X3

FIGURE 15D

Gate oxidation in array and support
Gate poly deposition in array and support
Block mask to protect support/etch gate poly in array/resist strip

Schematics of TOL with ARC planarization & height equalization between array and support
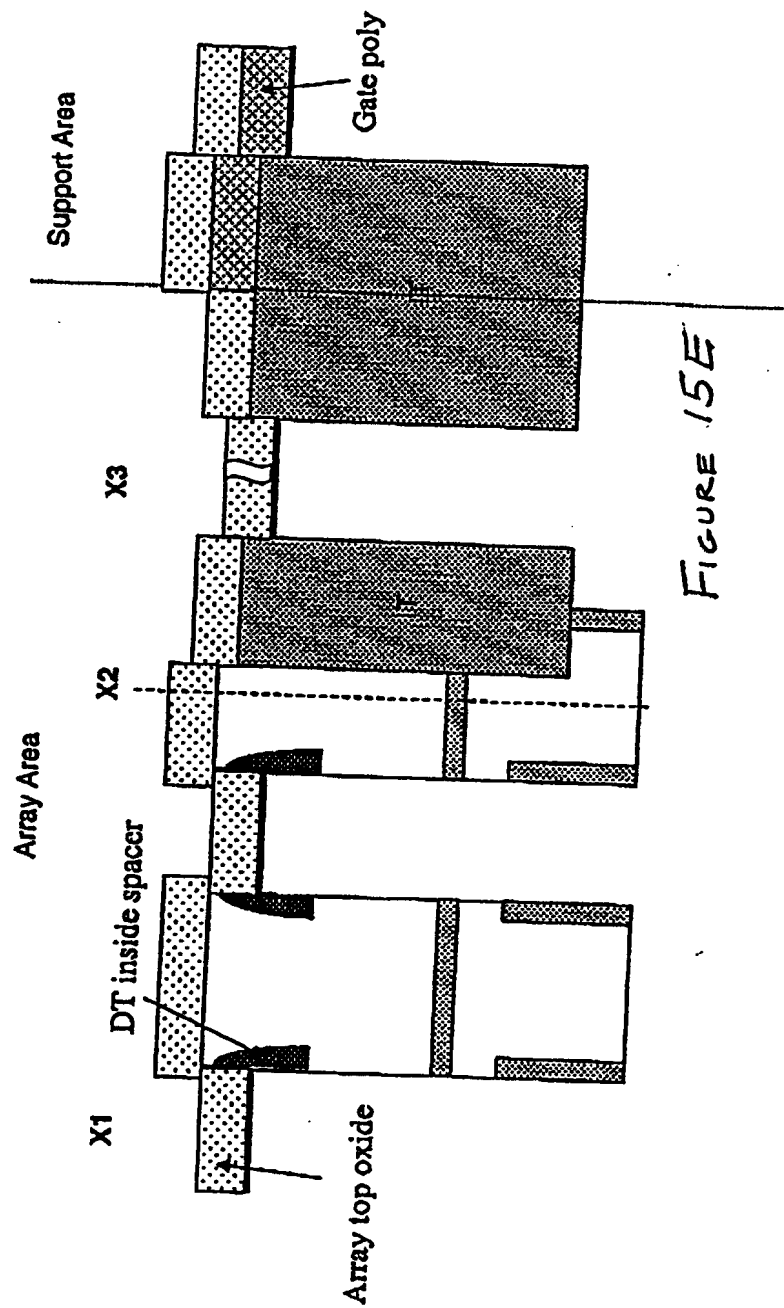
Array Area

Support Area

X1

X2

X3

Array top oxide

DT inside spacer

Gate poly

FIGURE 15E

Array top oxide deposition

Schematics of TOL with ARC planarization & height equalization between array and support

Array Area | Support Area

X1

DT inside spacer

X2
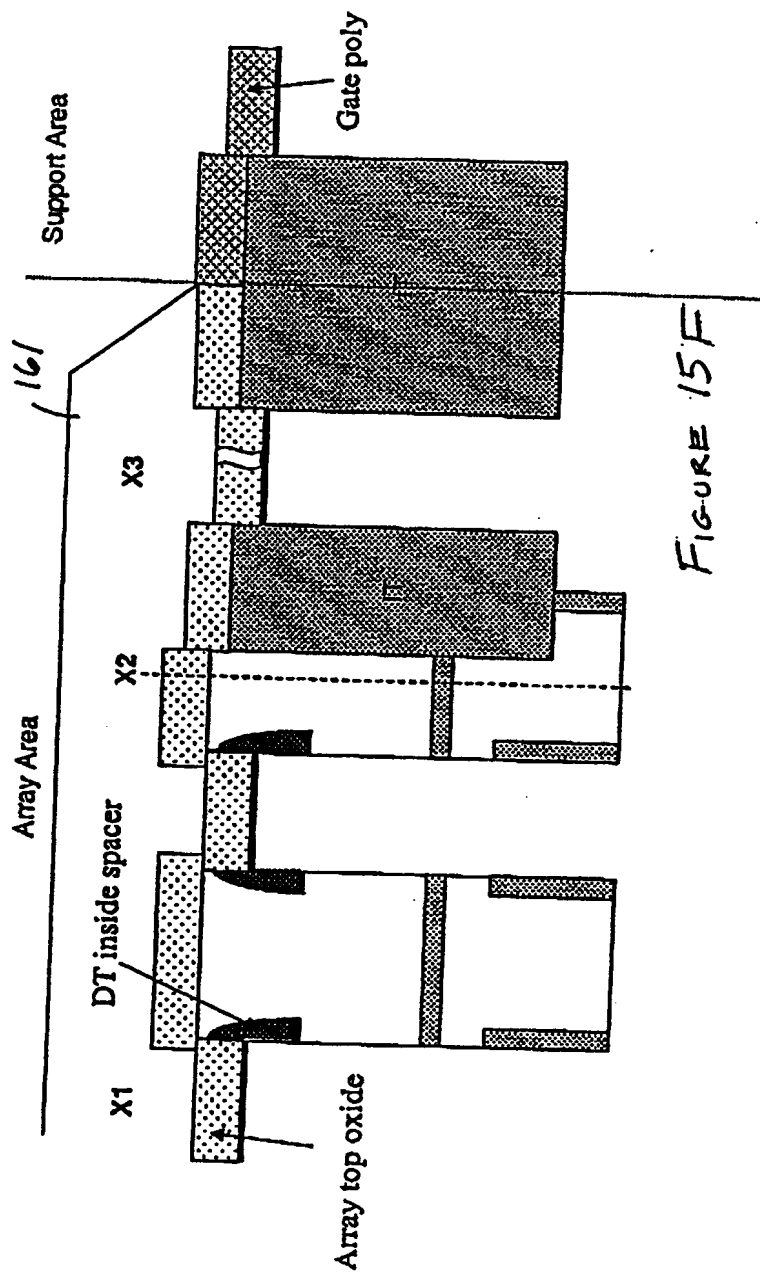
X3

161

Gate poly

Array top oxide

FIGURE 15F

Block mask to protect array/etch array top oxide in support to make the step height between array and support similar/resist strip (for Option II)

Schematics of TOL with ARC planarization & height equalization between array and support
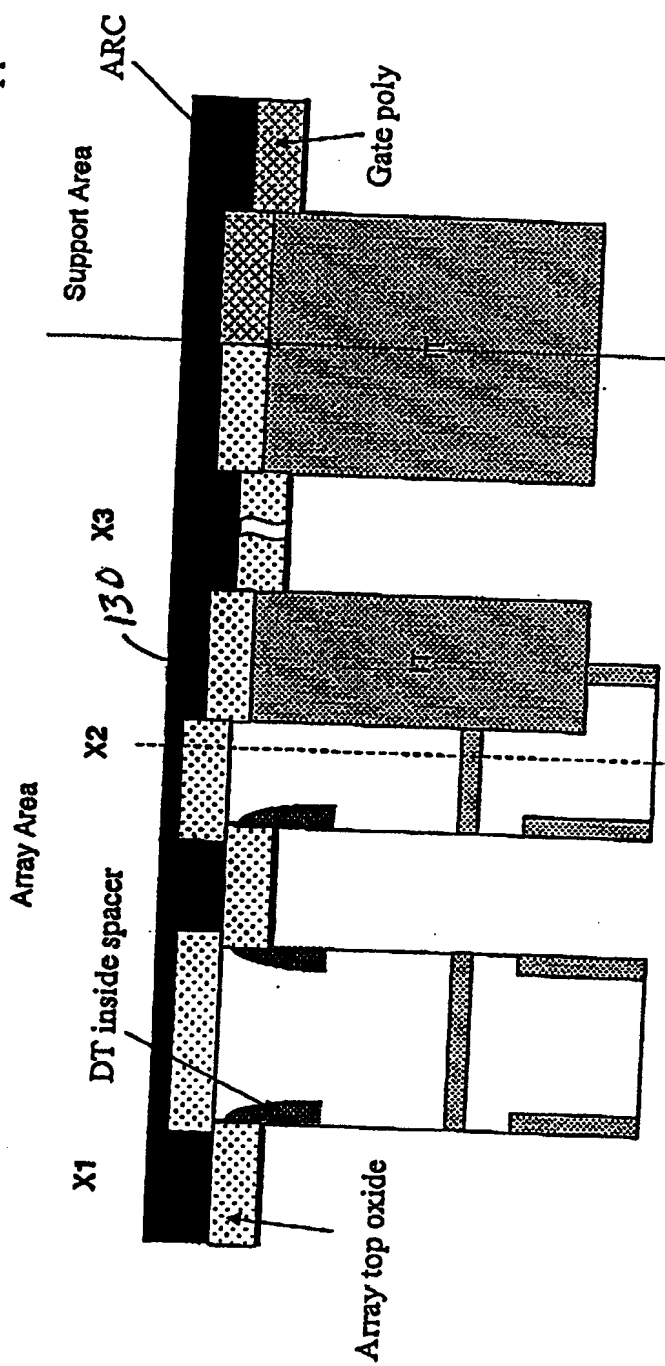
Array Area   Support Area

X1   DT inside spacer   X2   130 X3   ARC

Gate poly

Array top oxide
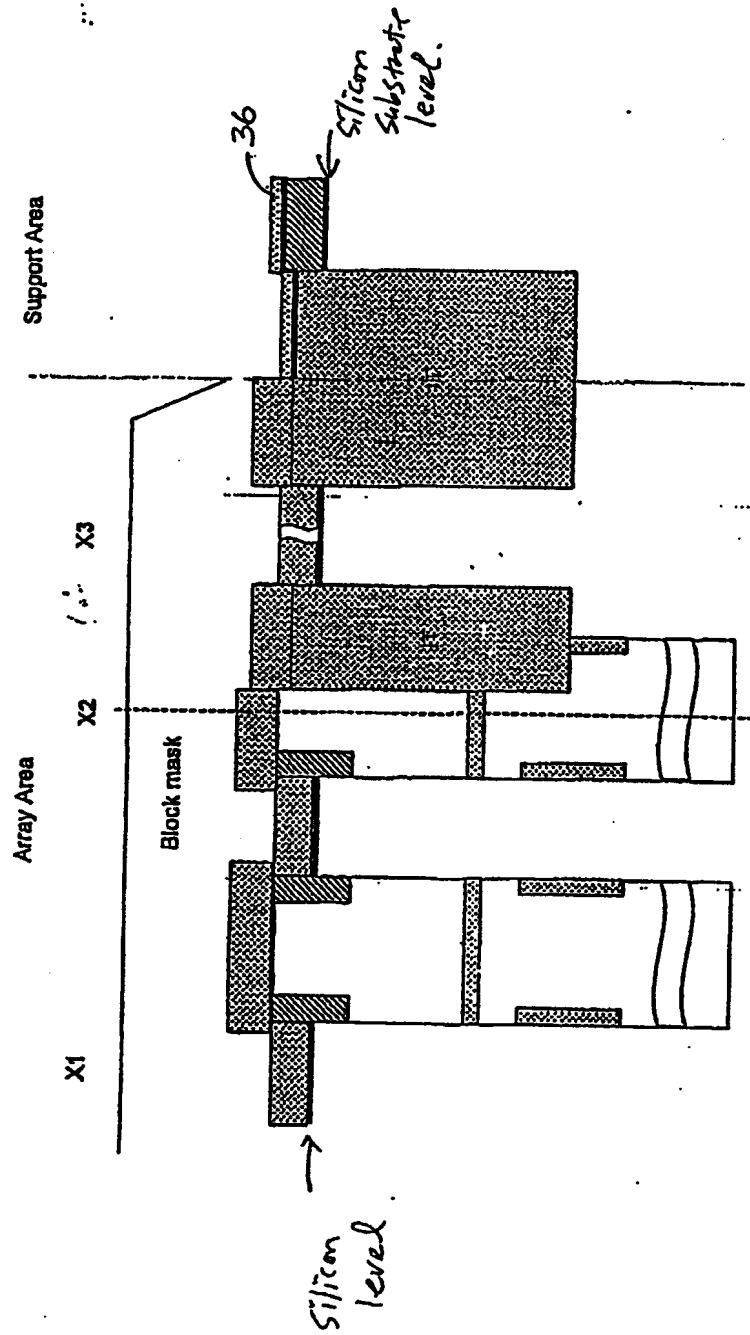
ARC deposition

$F_{IGURE} \, 15G$

FIGURE 16 - Block mask/oxide etch in support (in order to make the average step height in support same as that in array)/strip

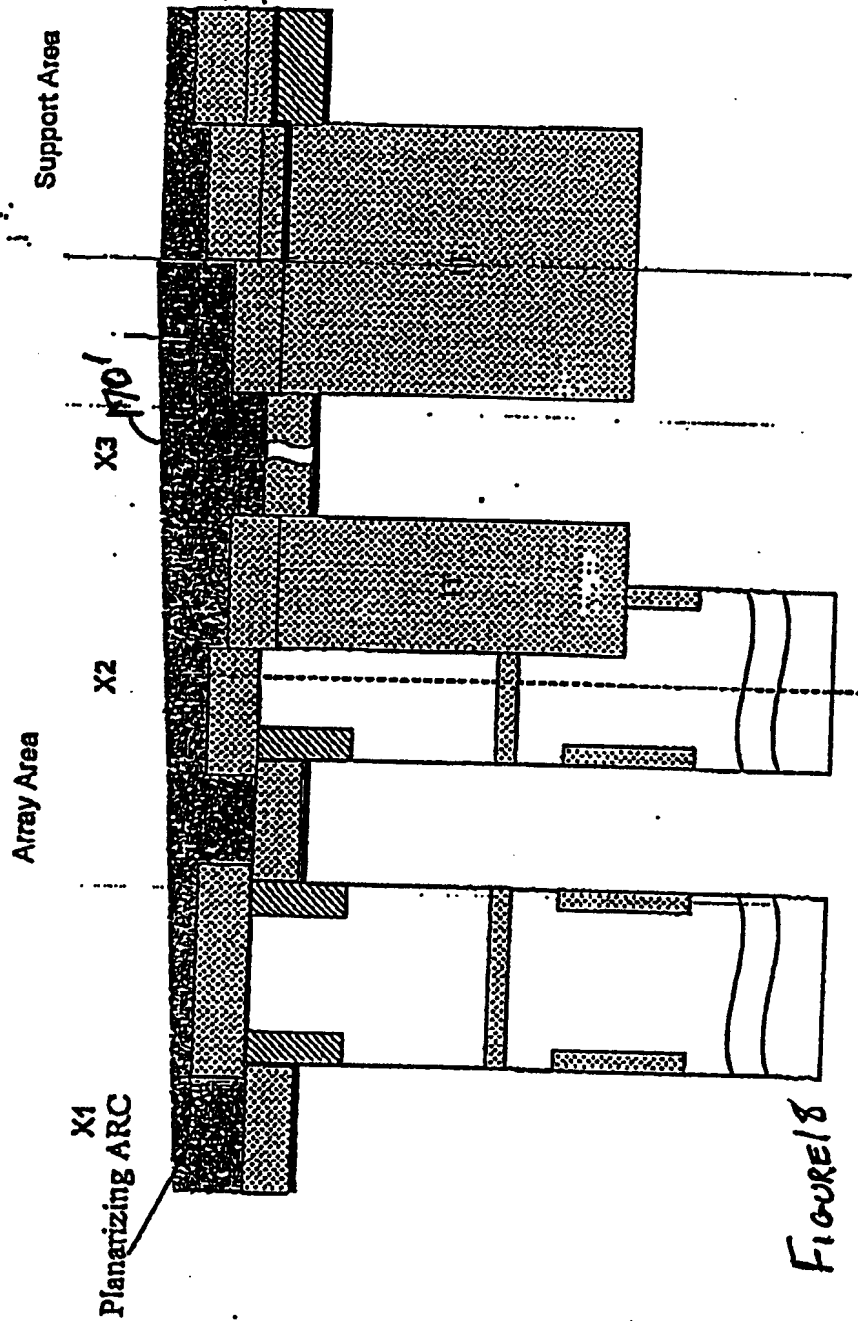Deok-kee Kim, Hiro Akatsu, Rama Divakaruni

IBM Confidential

Support Area

Array Area

Silicon Substrate level.

36

Silicon level.

Block mask

X1   X2   X3

Support Area

Array Area

Planarizing ARC
X1

X2

X3

ITO

FIGURE 17 – planarizing ARC dep (profile with block mask/oxide etch in support/strip)

Support Area

Array Area

X1
Planarizing ARC

X2

X3

170'

FIGURE 18

- Profile without block mask/oxide etch in support/resist strip (this is another disclosure - improved TOE)

Support Area

Array Area

X1   X2   X3

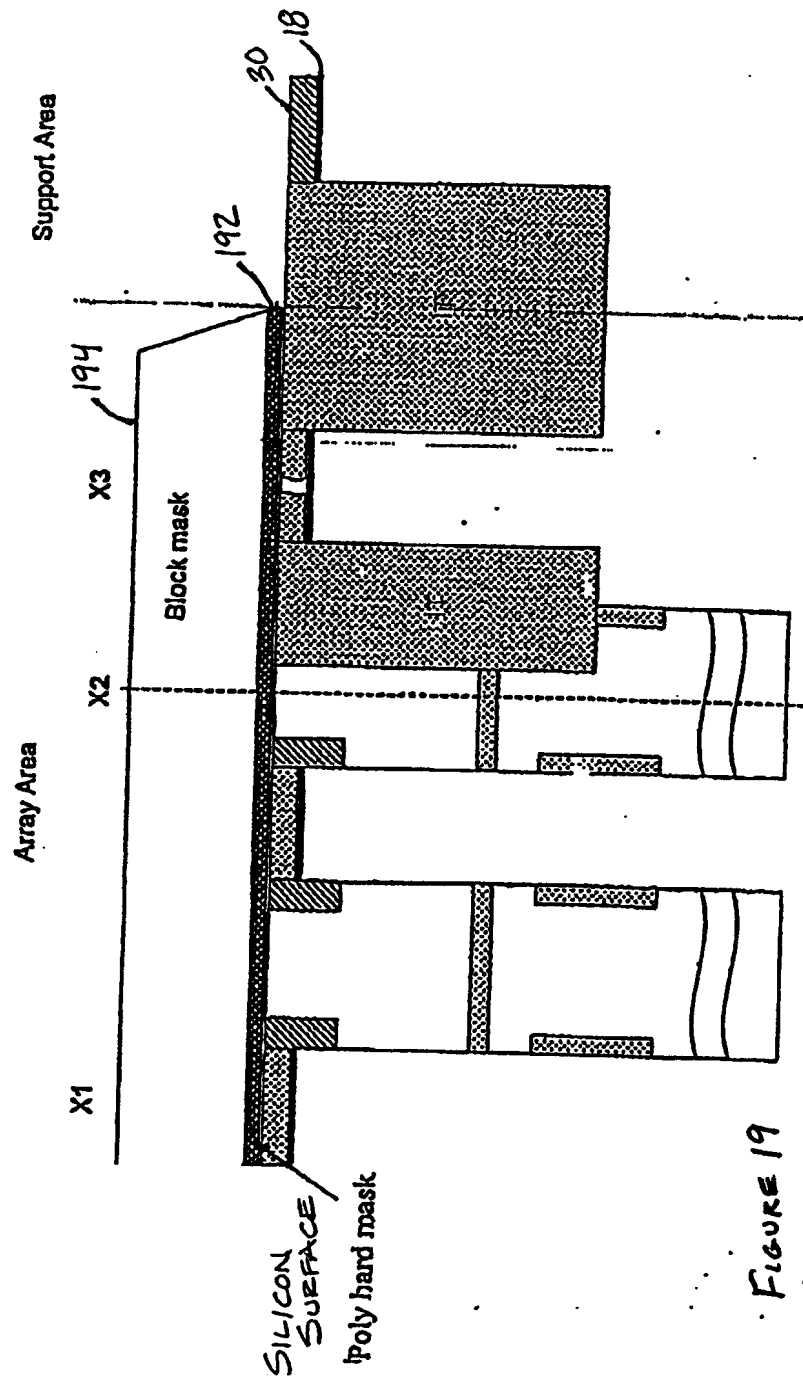Block mask

30
18
192
194

SILICON
SURFACE
Poly hard mask

FIGURE 19

Non-selective ARC assisted RIE (this step replaces chemical mechanical polishing, can be controlled by end point)
/ES poly dep/ES mask (block mask)/poly removal in support/strip

Support Area

192

200

202

X3

Array Area

X2

196

X1

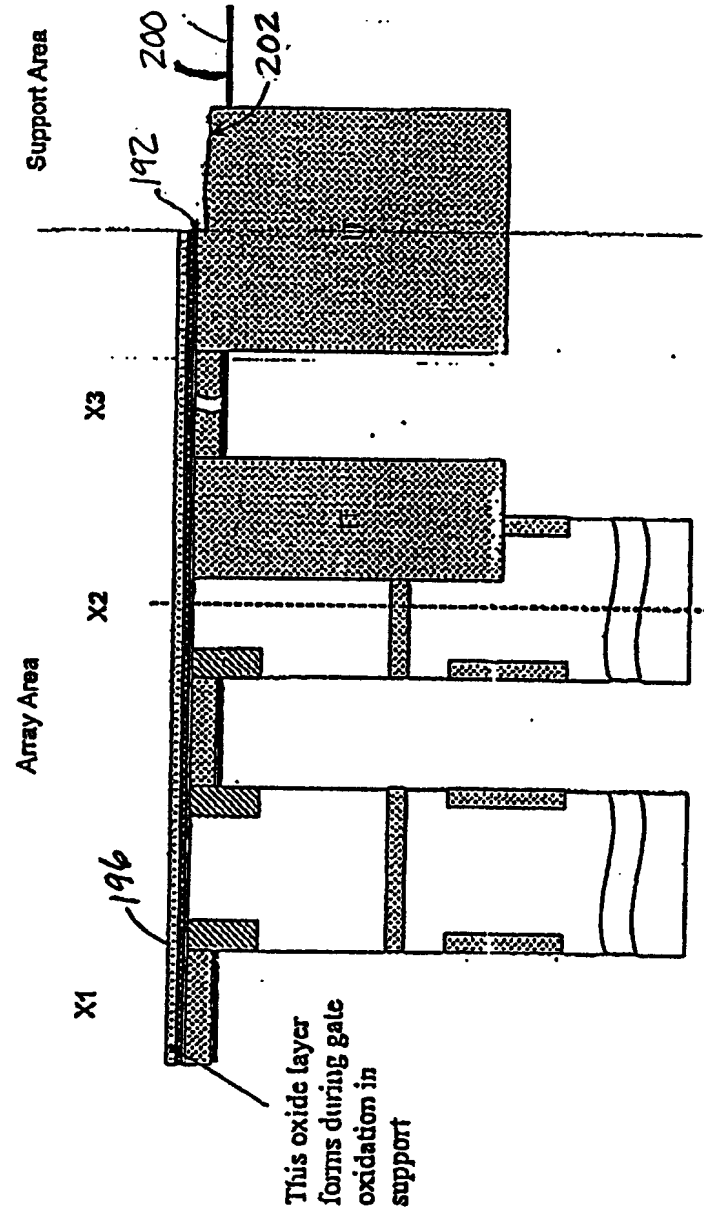This oxide layer forms during gate oxidation in support

FIGURE 20. Etch oxide, nitride liner & IT oxide to a desired height/Strip pad nitride in support/Pad oxide strip & sac ox growth in support/Support implants
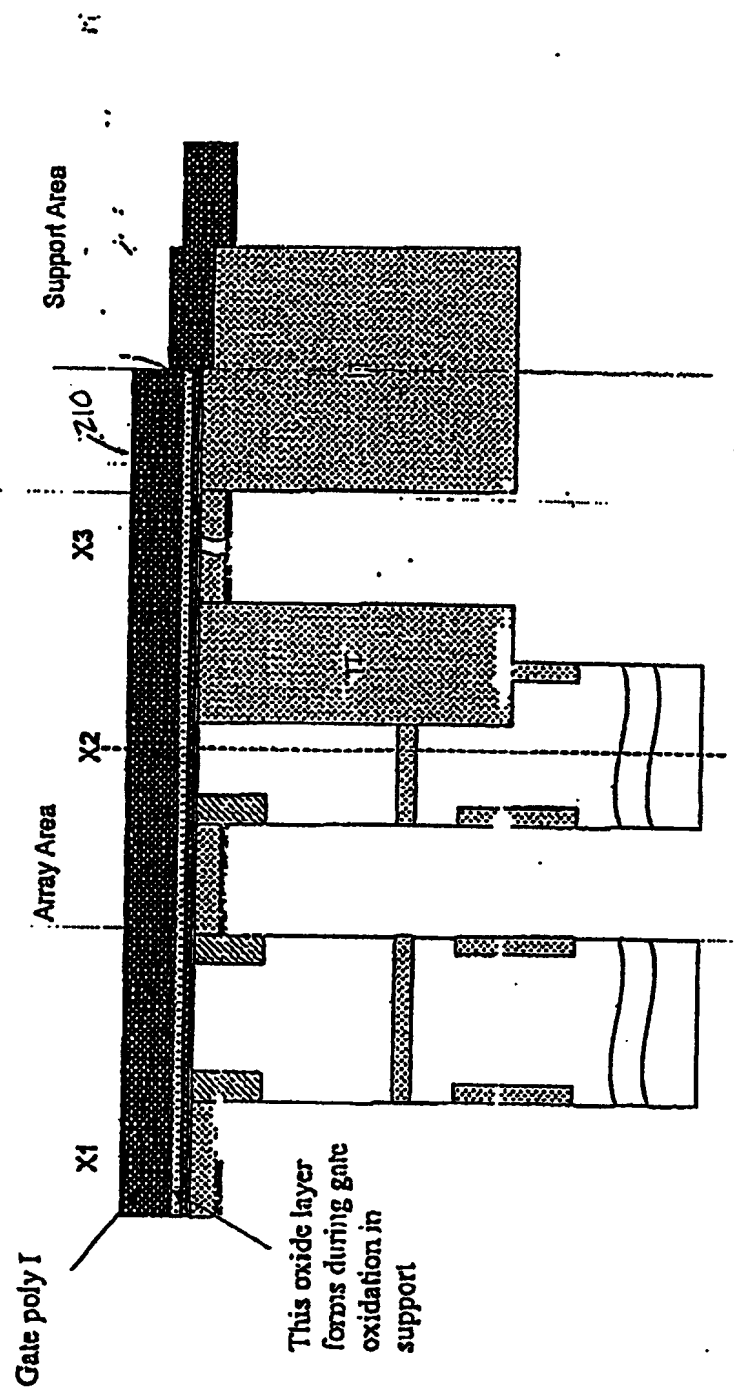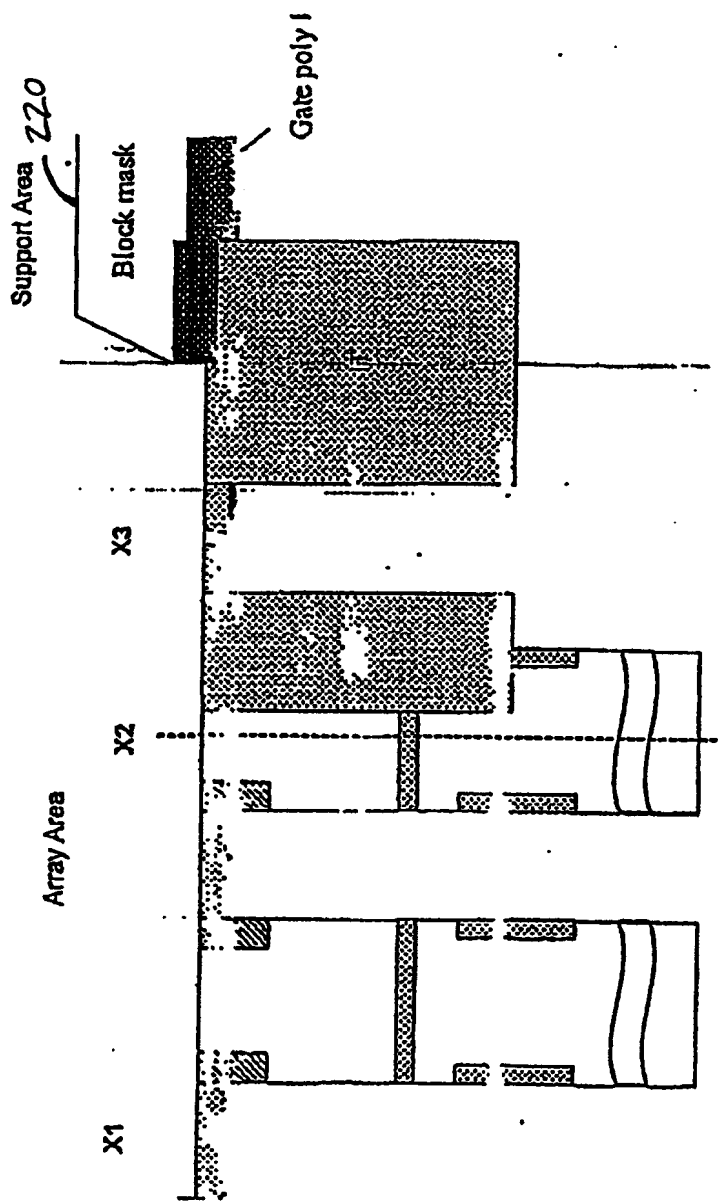
FIGURE 21 - Gate ox/Gate poly 1 dep

Support Area

Array Area

Gate poly I

This oxide layer forms during gate oxidation in support

X1 X2 X3

210

Figure 22 – Block mask/poly, oxide, poly etch in array/strip
Continue with WL's/BL's formation and BEOL processes